Introduction

Clock distribution is a significant design challenge for systems operating above 25MHz. The Micrel-Synergy Semiconductor PECL series of clock chips simplifies designs by significantly reducing clock skew — the source of most problems in high-speed clock distribution design. This application brief examines the various aspects of clock system design using a system design as an example.

Figure 1 shows an example of such a high-speed computer system with a clock subsystem. The system consists of a 32-bit CPU with a memory control subsystem, peripheral chips and a clock subsystem. The clock subsystem drives the various clock pins of the system. The clock subsystem consists of an ECL crystal oscillator (Xtal), an SY10E111 PECL clock distributor, and SY10H842 PECL-to-TTL clock drivers. The SY10E111 PECL clock distributor generates the primary clock signal and drives the SY10H842 PECL-to-TTL clock drivers.

Differential PECL signals, such as those used by the SY10E111 and SY10H842, have unique advantages for clock distribution systems. Differential PECL signals provide good noise rejection. Because they are differential and have low swing, they minimize EM radiation from the board; they can drive low impedance transmission line traces for minimum trace delay; they have equal rise and fall times which preserves the clock duty cycle; and, by exchanging the inputs to the PECL-to-TTL converter, one can obtain inverted clocks easily with minimum skew.

Synchronous digital systems — such as shown in Figure 1 — use the concept of a single clock coordinating the actions of all system components. In real systems, the low-to-high controlling clock edges do not happen at the same time. The difference in time between the rising edge of one clock pin and another is called clock skew. Clock skew is generated by differences in delay between the clock oscillator and the clock pins. This delay is a combination of the delay through different clock drivers and the time required for the clock to propagate down the PC board trace (known as trace delay).

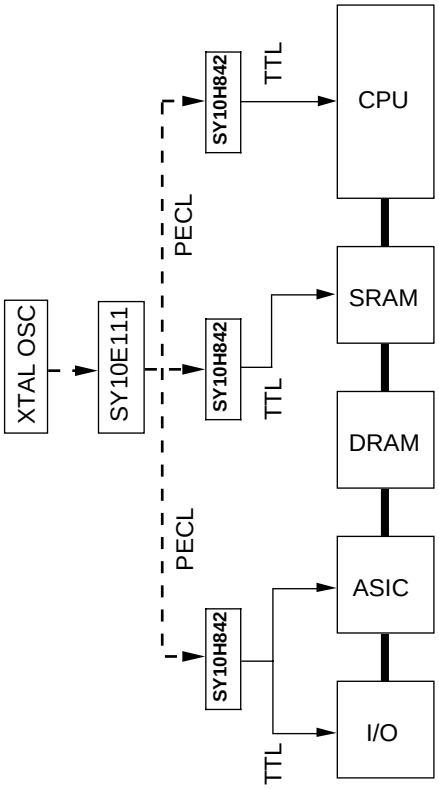

Figure 1. A 32-Bit Microprocessor System

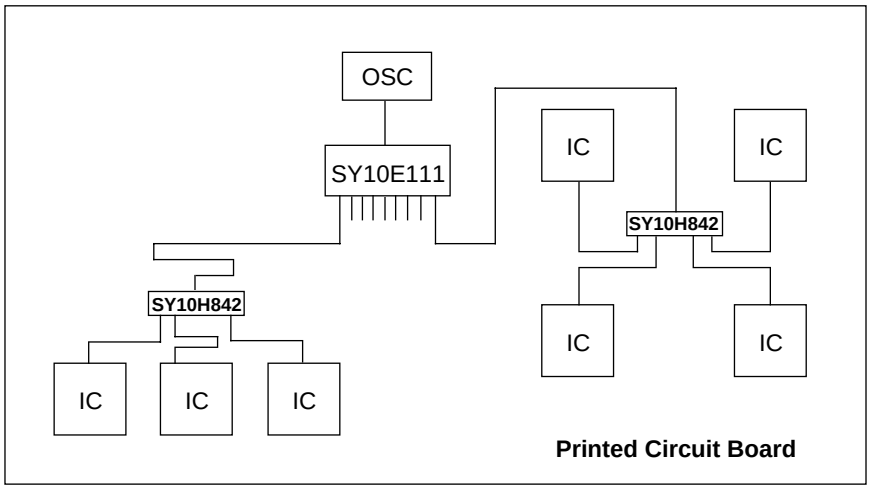

Figure 2. Clock Distribution Board Layout Example

Figure 2 shows what a board layout of the system of Figure 1 might look like. Note that the traces run in serpentine patterns to keep the trace lengths from the SY10E111 to the SY10H842s and from the SY10H842s to their IC loads equal in length.

The PECL Clock Chips

Figures 3 and 4 show block diagrams of the SY10E111 and SY10H842 PECL clock chips, respectively. The SY10E111 is a 1-in, 9-out PECL clock distributor chip. It multiplies the single clock input from the crystal oscillator into 9 copies for distribution to the SY10H842 chips. The SY10E111 has very low output-to-output skew (0.05ns) and low part-to-part skew (0.2ns). The SY10E111 is normally driven by the master clock source — the crystal oscillator in this case — and the SY10E111 outputs drive PECL-to-TTL clock drivers such as the SY10H842. The SY10E111 can also drive other SY10E111 chips. One can create large clock systems with low skew by using the first SY10E111 chip to drive other SY10E111 chips. A single SY10E111 generates 9 PECL clock outputs and up to 36 TTL outputs using SY10H842 PECL-to-TTL clock drivers. Two layers of SY10E111s can generate up to 81 PECL clock outputs and 324 TTL outputs. The SY10E111 is available in a 28-pin PLCC package. The PLCC package allows balanced lead lengths for low skew, and the plastic package minimizes propagation delay.

The SY10H842 is a 4-output PECL-to-TTL converter. The SY10H842 has low output-to-output skew for outputs in the same package (0.3ns) and for outputs in different packages (0.5ns). It has flow-through style pinouts for ease of layout and one TTL ground for each pair of outputs for low ground bounce noise. It is supplied in a 16-pin, low-inductance SOIC package.

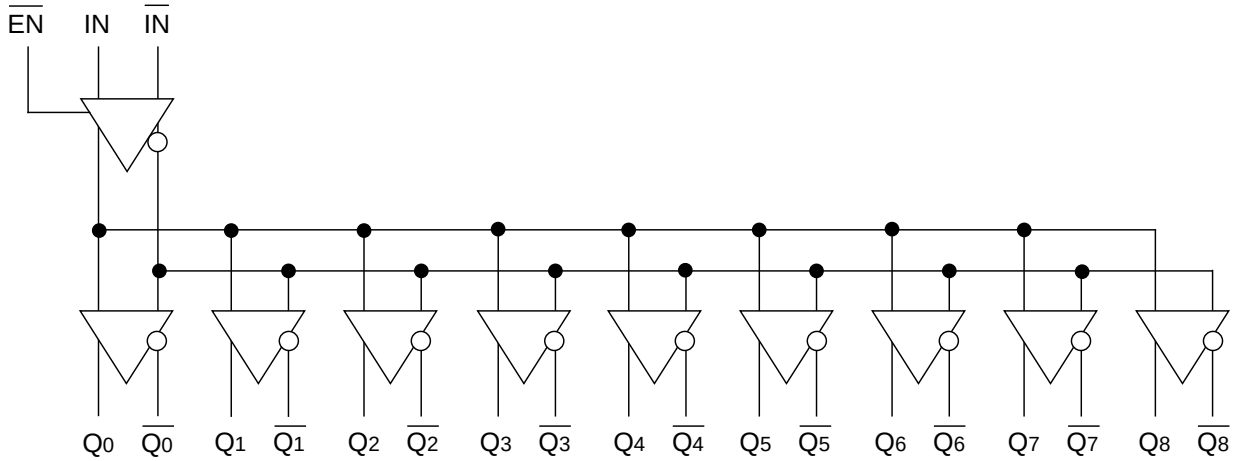

Figure 3. SY10E111 Block Diagram

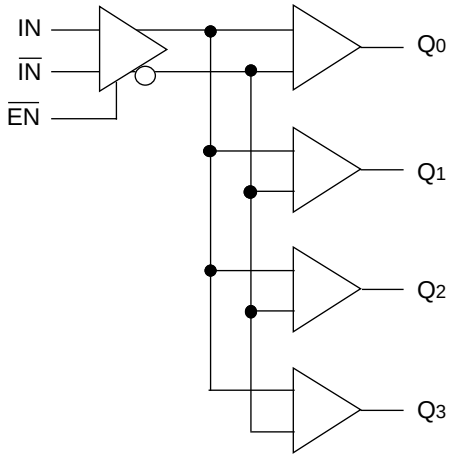

Figure 4. SY10H842 Block Diagram

The delay for the shortest and longest path for the system shown in Figure 1 are given in Table 1.

Delay Element	Skew	Value
SY10E111 Output-to-Output Skew, Max.	0.05	ns
Trace Delay, SY10E111-to-SY10H842, 3/4" Difference at 0.15ns/in	0.10	ns
SY10H842 Package-to-Package Skew, Max.	0.50	ns
Loading Delay, SY10H842, 5pF Difference at 1.5ns/50pF	0.15	ns
Trace Delay, SY10H842-to-Load, 3/4" Difference at 0.25ns/in	0.20	ns
Totals	1.00	ns

Table 1. System Clock Skew Example

Several variations of the SY10H842 are also available. The SY10H841 is a 4-output part, similar to the SY10H842, but has an input latch for holding the clock signal in a specified state. The SY10H843 is similar to the SY10H842 but has a pair of input latches for both the data and enable signals. It has a synchronous enable for stopping the clock without glitches or short pulse effects. The SY10H641 is a 9-output PECL-to-TTL converter in a 28-pin PLCC package. Note that all the PECL-to-TTL clock driver chips in a system design must be of the same type for the specified package-to-package skew specification to apply. All of the clock chips are available with either 10K PECL (e.g. SY10E111) or 100K PECL (e.g. SY100E111) signal level compatibility.

Calculating Skew

Clock skew is defined as the difference in time between the clock edges arriving at a pair of clock input pins. In a perfect system, all clock signals arrive at all the various clock input pins of the system at exactly the same time, and the skew is zero. In real systems, the edges do not arrive at exactly the same time and there is some skew. Clock skew exists because of differences in the delay paths from the master clock oscillator to the various clock input pins. Delay accumulates along each clock path and the delays for the various paths are not equal. The maximum clock skew for the system is the difference in delay between the shortest and longest delay paths.

We can calculate the skew for a system by calculating the differences in delay along the clock paths. In the clock system of Figure 1, each delay path consists of the following elements:

- Delay through the SY10E111
- Trace delay from the SY10E111 to the SY10H842
- Delay through the SY10H842
- Output delay of the SY10H842 due to capacitive loading
- Trace delay from the SY10H842 to the clock input pin

The delay from the master clock oscillator to the SY10E111 does not contribute to clock skew because it is exactly the same for all clock paths: all clocks share this delay path element. The SY10E111 data sheet specifies the maximum skew between outputs on the same chip to be less than 0.05ns. Small clock systems such as this example use a single SY10E111 which adds only 0.05ns to the total skew. Large clock systems using one SY10E111 driving other SY10E111s have 0.05ns of skew for the first SY10E111, plus 0.20ns of package-to-package skew for each layer of SY10E111s.

Trace delay from the SY10E111 to the SY10H842 is determined by the length of the clock trace on the printed circuit board, the material of the board, and the capacitive loading of the SY10H842 input. For glass epoxy printed circuit cards, the unloaded trace delay is 0.144ns/inch. The capacitive loading of the input pins of the SY10H842 increases this delay. A figure of 0.15ns/inch is used in this example.

The skew for outputs within a single SY10H842 is 0.30ns; however, this example uses more than one chip so the chip-to-chip skew value of 0.50ns must be used.

The SY10H842 is specified with a 50pF load. Good design practice dictates that each SY10H842 TTL output drive only one load — typically between 5 and 10pF. The SY10H842 loading factor is 1.5ns per 50pF additional capacitance. If the loads on the outputs differ by 5pF, a corresponding skew of 0.15ns is introduced.

The final element of skew is trace delay from the SY10H842 to the load (i.e., the clock input pin being driven). The TTL trace is typically more heavily loaded than the PECL lines from the SY10E111 to the SY10H842. This means that the TTL trace delay per inch of trace is larger than the 0.144ns/inch of unloaded traces. A typical number is 0.25ns/inch. This number is used in the calculations, and the traces are assumed to be from 1 1/4 inch to 2 inches long from the SY10H842 to the various clock input pins.

The total clock skew for the system is the sum of the skews of the various elements. The total skew in this example is 1.00ns. Note that 0.30ns of this delay is due to trace length differences of 3/4 inch on the PECL and 3/4 inch on the TTL traces. Also, 0.15ns of skew is due to 5pF difference in loading on the various outputs. These values are affected by the system design and board layout. If these differences could be cut in half, for example, the skew could be cut by 0.23ns, reducing the total skew to 0.77ns. The rule of thumb for maximum skew is 10% of a clock cycle. For a 100MHz system, the maximum skew is 1ns. Utilizing Micrel-Synergy's low skew SY10E111 and SY10H842 PECL clock distribution system, this maximum skew requirement can easily be met.

System Clock Skew Requirements

Now that we know how to calculate clock skew, we need to know how to calculate the system clock skew requirements (i.e., the system clock skew design budget). Clock skew is the main design parameter in high-speed clock systems. System timing determines clock skew requirements. The system timing diagram of Figure 5 shows the effect of clock skew. In this diagram, we have a data source, such as the CPU, driving a receiver such as an I/O device. The CPU puts data on the bus that is received and clocked in by the I/O device. The CPU makes the data valid on the bus for a set-up time, t_{BS}, before the clock. The CPU holds it valid for a hold time, t_{BH}, after the clock. The I/O device requires that data be present at its inputs for a set-up time, t_{IS}, before the clock, and that it be held valid for a hold time, t_{IH}, after the clock. The timing design margin is the amount of excess time the data is valid before the minimum required set-up time and after the minimum required hold time. The design margin for data set-up is ($t_{BS} – t_{IS}$); for data hold, it is ($t_{BH} – t_{IH}$).

Let us consider the case where the I/O device receives an early version of the clock, called I/O Clock in Figure 5. This clock is early with respect to the CPU clock, the source of the data on the bus. The I/O device input set-up and hold window is relative to its clock. In Figure 5, I/O Clock has moved the I/O input set-up and hold window early enough in the cycle that the data on the bus is not yet valid and its input set-up requirements are violated. A similar situation occurs if the I/O device clock is late. If the I/O clock is too late, the I/O input hold requirement is violated.

Excessive clock skew violates input set-up or hold requirements for control or data signals. The problem is also relative. The clock at the receiver is early or late with respect to the clock at the driver. In the case shown, the CPU is driving an I/O device, and the I/O device clock is early with respect to the CPU clock. If the I/O device is driving the CPU on the next cycle, the CPU clock will be late with respect to the I/O device.

The difference in timing between two clock signals is called clock skew. The difference in time between the rising edges of CPU Clock and I/O Clock in Figure 5 is the clock skew, t_{SKEW}. The maximum value of skew is determined by the set-up time margin ($t_{BS} – t_{IS}$) for I/O Clock arriving early, to the hold time margin ($t_{BH} – t_{IH}$) for I/O Clock arriving late. Since clock skew is relative, all combinations of data output set-up and hold and data input set-up and hold are considered. The allowable clock skew is the minimum of these combinations of set-up and hold margins.

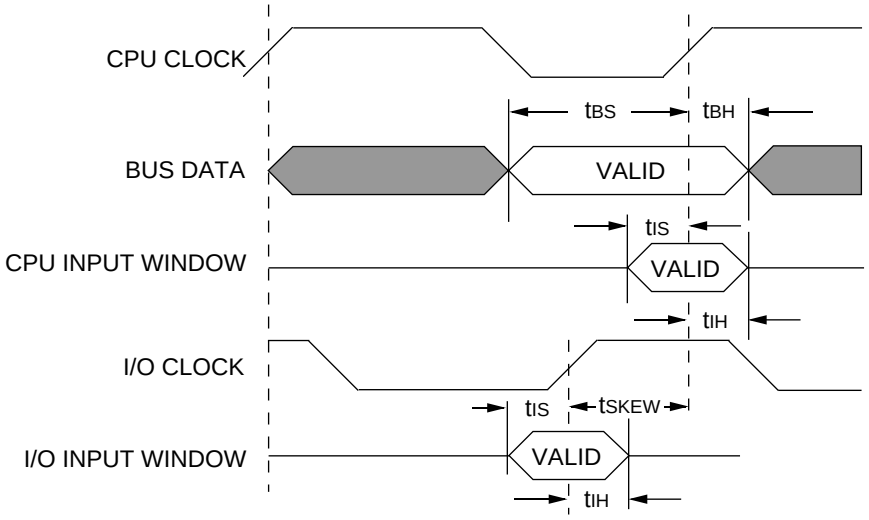

Figure 5. Clock Skew Timing Diagram

Designing With Micrel-Synergy PECL Clock Distribution Chips

Designing clock distribution systems with the Micrel-Synergy PECL series of clock chips is straightforward, as shown above. The simplicity of system design is a result of several advantages of the PECL/TTL clock distribution system approach. The elements of clock skew in the PECL/TTL approach are typically much lower and more predictable than in TTL-only designs.

The delay through a PECL chip is typically 1/5 to 1/10 the corresponding delay through a TTL chip. The SY10E111 PECL clock distributor shown in Figure 3 has a propagation delay of 0.63ns compared to the TTL 74FCT244D at 3.8ns. Lower propagation delay also means lower skew. The PECL SY10E111 has very low on-chip skew (0.05ns) and relatively low chip-to-chip skew (0.20ns) as compared to TTL buffer chips which have typical skews of 1.0ns and 2.5ns, respectively. The speed of PECL technology also applies to the SY10H842 PECL/TTL clock driver. It has a maximum propagation delay of 3.5ns, a maximum output-to-output skew of 0.3ns, and a maximum part-to-part skew of only 0.5ns.

Differential PECL signals minimize the propagation delay per inch of trace between the SY10E111 clock distributor and the SY10H842 PECL/TTL clock drivers. The delay per inch of trace on a PC board is 0.144ns/inch for G-10 glass epoxy boards with a dielectric constant of 4.7. This represents the minimum propagation delay per inch of trace. Adding capacitance to the trace increases this delay per inch value. Reducing the transmission line impedance of the traces reduces the effect of this capacitance. PECL chips such as the SY10E111 are designed to drive low impedance, 50 ohm transmission lines. This low impedance minimizes the effect of the SY10H842 PECL input capacitance at the receiving end of the trace, which keeps the propagation delay per inch of the transmission line low. This combination allows the SY10E111 and SY10H842 combination to achieve a 0.15ns/inch delay.

Differential PECL signals also provide high noise immunity compared to single-ended TTL signals. Crosstalk, ground and power noises tend to affect both PECL signals in the same way. The result is common mode noise on the signal pair. This common mode noise is rejected by the differential PECL input. The result is a clean signal as seen by the PECL inputs. This means no clock jitter due to noise, preservation of clock duty cycle, and no problem with V_{CC} variations from one part of the board to another. PECL signals for clock distribution also mean low EM radiation because of the lower voltage swing and the fact that voltages and currents of differential PECL transmission lines cancel each other for minimum radiation.

Differential PECL signals provide a third, unique capability: low skew inverted clocks. By simply exchanging the PECL signals to a selected PECL-to-TTL clock driver, the output clock signals output from that driver are inverted with respect to other clocks in the system.

With these advantages in mind, the following is a set of PECL/TTL clock system design recommendations:

- Use the PECL SY10E111-to-SY10H842 lines for clock routing for minimum delay and noise.
- Use 50 ohm stripline (internal) traces for the PECL lines. This gives 50 ohm lines in small size.
- Make the PECL traces equal length for minimum skew. Each inch difference is 0.15ns of skew.
- Put the PECL/TTL converters near their loads: keep the TTL traces short for low noise and delay.
- Use one TTL driver per load and keep the loads as equal as possible for minimum skew and noise.

PECL Clock Distribution Line Termination

The PECL lines from the SY10E111 to the SY10H842s are transmission lines for traces longer than one inch. These traces must be terminated at the SY10H842 end in the characteristic impedance of the transmission line; otherwise, there will be signal reflection and noise which can distort the clock signal. The SY10E111 is designed to drive 50Ω transmission lines. One can design printed circuit traces to be 50Ω transmission lines by properly sizing the width of the trace (see Appendix 1). There remains the requirement of terminating each of the pair of lines in its 50Ω impedance.

One can terminate the differential PECL signals with 50Ω resistors to a terminating voltage of 3V (i.e., 2.0V below V_{CC}). This requires a separate terminating voltage power supply. A simpler method is to use an RC network, as shown in Figure 6. The RC network of Figure 6 takes advantage of the fact that the signals are differential and always opposite in phase. The two termination resistors, Rt, are connected to a common bias resistor, Rb. The bias resistor provides the current that would normally be supplied by a 3.0V terminating voltage power supply.

The correct size for the Rb bias resistor is 107Ω; a 110Ω resistor will work. The decoupling capacitor, Ct, keeps the terminating voltage constant while the signals are switching so that each line sees a 50Ω terminating impedance. The RC time constant of Ct and the terminating resistors would be 10 times the round trip delay of the longest transmission

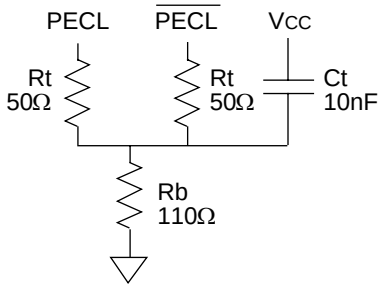

Figure 6. PECL Resistor Termination

line. If this is 5ns, the RC time constant should be larger than 50ns and Ct should be larger than (50ns/25Ω) = 2nF = 200pF. A value for Ct of 10,000pF (0.01µF) will work nicely. Note that Ct is connected to VCC. This is because PECL signals are generated relative to VCC. The VCC plane for TTL is the “ground” plane for PECL.

APPENDIX 1

Printed Circuit Trace Characteristics

The geometry of printed circuit traces and the dielectric constant of the printed circuit board material holding them determine their transmission line characteristics. Figure A1 shows the two major trace types used on PC boards: the Surface Micro Stripline, and the Internal Stripline. Table A1 gives the equations for calculating their characteristics and some example values. You can use these equations in a spreadsheet to calculate the propagation delays on your circuit board, and you can use the example values to debug the spreadsheet.

Adding load capacitance to a trace increases its effective distributed capacitance. This decreases its impedance and increases the delay per inch. The equations in Table A1 give the effective termination impedance and trace delay for single traces with capacitive loading.

Table A1 gives the unloaded characteristic impedance, propagation delay per inch, capacitance per inch and inductance per inch for various combinations of trace width and board thickness for both Surface Micro Stripline and Internal Stripline traces. Surface traces are on the board surface over a ground plane. The board thickness (d) is the thickness between the trace and the ground plane. A 0.012" thickness corresponds to the surface trace of a typical 6-layer board. Internal traces are between ground planes. The board thickness(s) is the distance between the two ground planes and assumes that the trace is centered between them. The 0.026" thickness is for an internal trace on a 6-layer board where the 0.026" is the distance from a center ground plan to the surface layer of the board. This 0.026" thickness corresponds to 2 times layer spacing (d, as in Micro Stripline), and trace thickness (t).

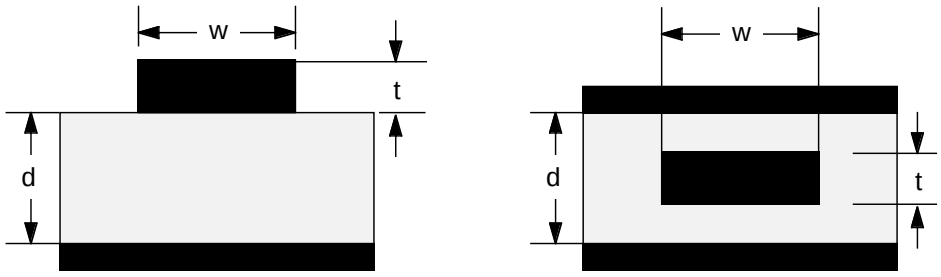

Figure A1. Printed Circuit Trace Geometries

Surface Micro Stripline

Parameter	Symbol	Unit	Equation	Example
Dielectric Constant	Er	—	—	4.7
Board Thickness	*d*	inch	—	0.012
Trace Width	*w*	inch	—	0.010
Trace Thickness	*t*	inch	—	0.002
Impedance	Z0	ohms	$\frac{87}{\sqrt{Er + 1.41}} \text{Ln} \frac{5.98\,d}{0.8\,w + t}$	69.36
Delay/Inch	t_{PDZ}	ns/in	$0.08475 \sqrt{0.475\,Er + 0.67}$	0.144
Capacitance/Inch	Cz	pF/in	$1000 \frac{t_{PDZ}}{Z\,0}$	2.08
Inductance/Inch	Lz	nH/in	$t_{PDZ} Z\,0$	9.99
Capacitive Load	Cload	pF	—	3.7
Z with Distributed Capacitive Loading	Z	ohms	$Z\,0 \sqrt{\frac{Cz}{Cz + Cload}}$	41.61
t_{PD}/in with Distributed Capacitive Loading	t_{PD}	ns/in	$t_{PDZ} \sqrt{\frac{Cz + Cload}{Cz}}$	0.24

Internal Stripline

Parameter	Symbol	Unit	Equation	Example
Dielectric Constant	Er	—	—	4.7
Board Thickness	*d*	inch	—	0.026
Trace Width	*w*	inch	—	0.010
Trace Thickness	*t*	inch	—	0.002
Impedance	*Z*0	ohms	$\frac{60}{\sqrt{Er}} \text{Ln} \frac{4d}{0.536\pi w + 0.67\pi t}$	44.278
Delay/Inch	t_{PDZ}	ns/in	$.08475 \sqrt{Er}$	0.1837
Capacitance/Inch	Cz	pF/in	$1000 \frac{t_{PDZ}}{Z\,0}$	4.149
Inductance/Inch	Lz	nH/in	$t_{PDZ} Z\,0$	8.134
Capacitive Load	Cload	pF	—	3.7
Z with Distributed Capacitive Loading	Z	ohms	$Z\,0 \sqrt{\frac{Cz}{Cz + Cload}}$	32.192
t_{PD}/in with Distributed Capacitive Loading	t_{PD}	ns/in	$t_{PDZ} \sqrt{\frac{Cz + Cload}{Cz}}$	0.253

Table A1. Transmission Line Characteristics for Various Traces

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