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TUTORIAL 5133

Power-Supply Solutions for Altera FPGAs

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Abstract: Field-programmable gate arrays (FPGAs) are used in a wide variety of applications and end markets, including digital signal processing, medical imaging, and high-performance computing. This application note outlines the issues related to powering FPGAs. It also discusses Maxim's solutions for powering Altera® FPGAs.

Introduction

Field-programmable gate arrays (FPGAs) are used in a wide variety of applications and end markets, and they have been gaining market share over ASICs due to their excellent design flexibility and low engineering costs. Power-supply design and management for FPGAs is an important part of the overall application. This article discusses ways to overcome some of the power-supply design challenges and explains the trade-offs between cost, size, and efficiency. Maxim's solutions for Altera® FPGAs are also presented.

FPGA Overview

FPGAs are programmable devices consisting of an array of configurable logic blocks (CLBs) connected through programmable interconnects. These CLBs typically comprise various digital logic components, such as lookup tables, flip-flops, multiplexers, etc. Other components of an FPGA include input/output pin driver circuits (I/Os), memory, and digital-clock management (DCM) circuits. Modern FPGAs integrate features that include FIFO and error correction code (ECC) logic, DSP blocks, PCI Express® controllers, Ethernet MAC blocks, and high-speed gigabit transceivers (**Figure 1**).

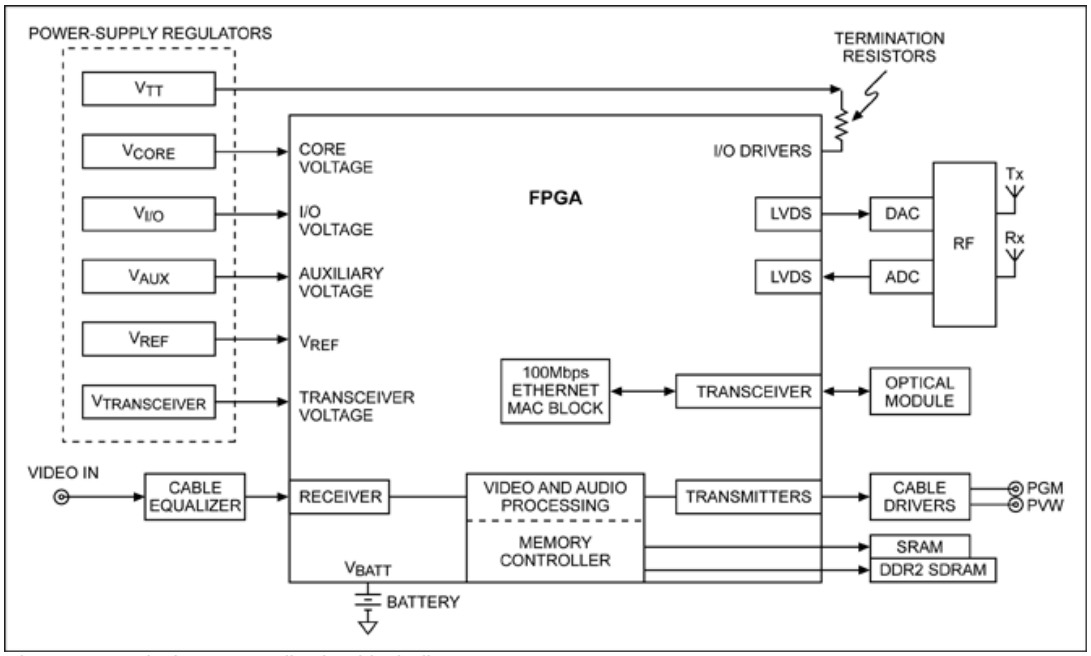


Figure 1. A typical FPGA application block diagram.

System-Level Power-Supply Architecture for FPGA Applications

Most high-performance/high-power FPGA applications in communications applications are built on plug-in cards that are powered by a 48V backplane. A two-stage intermediate bus architecture (IBA) is typically used in these applications for the individual cards (**Figure 2**). The first stage is a step-down converter that converts the 48V to an intermediate voltage, such as 12V or 5V. The plug-in-cards are often isolated from each other for safety reasons, and to eliminate the possibility of current loops and interference between the cards. The second stage of the IBA is to convert the intermediate voltage to multiple lower DC voltages, using nonisolated regulators known as "point-of-load" (POL) regulators. FPGAs used in computing, industrial, and automotive applications typically derive their power from a 12V to 24V nonisolated supply.

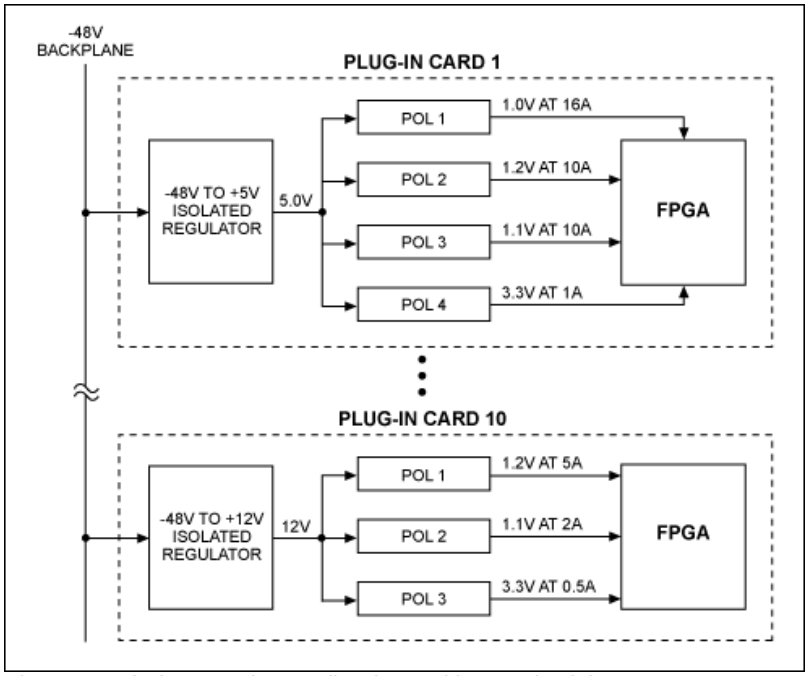


Figure 2. Typical 2-stage intermediate bus architecture (IBA) for FPGAs.

POL Regulators

POLs are high-performance regulators whose V_{OUT} rails are placed close to their respective loads. This helps solve the difficulties of high-transient-current demands and the low-noise requirements of high-performance semiconductor devices like FPGAs. The application-level parameters to be considered when designing a POL are:

- Cost
- Size
- Efficiency

The priority assigned to each of the above parameters often depends on the end market. Thus, each solution should be considered independently. For example, industrial and medical markets tend to favor size over cost, while wireless applications generally favor cost over size. Efficiency is particularly important to applications that run on batteries, and consumer applications are very conscious of all three parameters. The required efficiency usually determines what kind of DC-DC regulator is used, either low-dropout linear regulators or switch-mode power supplies.

Low-Dropout Linear Regulators (LDOs)

LDOs are relatively simple to implement, inexpensive, and produce very little noise. The major drawback with LDOs is their poor efficiency, which depends on the ratio of V_{OUT} to V_{IN}. For example, an LDO with V_{IN} = 3.3V and V_{OUT} = 1.2V has only 36% efficiency. The power difference is dissipated as heat.

Switch-Mode Power Supplies (SMPS)

SMPSs are typically > 90% efficient but are more difficult to implement than LDOs. They also conduct and radiate more noise when compared with LDOs.

LDOs are typically considered for applications with relatively low power requirements. SMPSs are used in higher-power applications due to their better efficiency, an important parameter for thermal management and reliability. Higher efficiency results in lower device temperatures, which improves reliability and reduces the overall solution size through smaller heatsink requirements.

Typical FPGA Power Requirements

A good example of a high-performance device is the Altera Stratix® V FPGA. **Table 1** shows the power-supply requirements for this part.

Table 1. Recommended Operating Conditions for the Altera Stratix V Power Supplies*

Power Supply	Description	Voltage (V, min)	Voltage (V, typ)	Voltage (V, max)
V_{CC}	Core voltage and peripheral circuitry power supply	0.82	0.85	0.88
V_{CCPT}	Power supply for programmable power technology	1.45	1.5	1.55
V_{CCAUX}	Auxiliary supply for the programmable power technology	2.375	2.5	2.625
V_{CCPD}	I/O predriver (3.0V) power supply	2.85	3.0	3.15
	I/O predriver (2.5V) power supply	2.375	2.5	2.625
V_{CCIO}	I/O buffers (3.0V) power supply	2.85	3.0	3.15
	I/O buffers (2.5V) power supply	2.375	2.5	2.625
	I/O buffers (1.8V) power supply	1.71	1.8	1.89
	I/O buffers (1.5V) power supply	1.425	1.5	1.575
	I/O buffers (1.35V) power supply	1.283	1.35	1.45
	I/O buffers (1.25V) power supply	1.19	1.25	1.31
	I/O buffers (1.2V) power supply	1.14	1.2	1.26
V_{CCPGM}	Configuration pins (3.0V) power supply	2.85	3.0	3.15
	Configuration pins (2.5V) power supply	2.375	2.5	2.625
	Configuration pins (1.8V) power supply	1.71	1.8	1.89
V_{CCA_FPLL}	PLL analog voltage-regulator power supply	2.375	2.5	2.625
V_{CCD_FPLL}	PLL digital voltage-regulator power supply	1.45	1.5	1.55
V_{CCBAT}	Battery back-up power supply (for design security volatile key register)	1.2	—	3.0
Transceiver GX and GS Power Supplies				
V_{CCA_GXBL}**	Transceiver high-voltage power (left side)	2.85, 2.375	3.0, 2.5	3.15, 2.62
V_{CCA_GXBR}**	Transceiver high-voltage power (right side)			
V_{CCHIP_L}	Transceiver HIP digital power (left side)	0.82	0.85	0.88
V_{CCHIP_R}	Transceiver HIP digital power (right side)			
V_{CCHSSI_L}	Transceiver PCS power (left side)	0.82	0.85	0.88
V_{CCHSSI_R}	Transceiver PCS power (right side)			
V_{CCR_GXBL}	Receiver power (left side)			

		0.82, 0.95	0.85, 1.0	0.88, 1.05
V_{CCR_GXBR}	Receiver power (right side)			
V_{CCR_GXBL}	Transmitter power (left side)	0.82, 0.95	0.85, 1.0	0.88, 1.05
V_{CCT_GXBR}	Transmitter power (right side)			
V_{CCH_GXBL}	Transmitter output buffer power (left side)	1.425	1.5	1.575
V_{CCH_GXBR}	Transmitter output buffer power (right side)			

*For the latest information on the Altera Stratix V, visit www.altera.com/products/devices/stratix-fpgas/stratix-v/stxv-index.jsp.
**This supply must be connected to 3.0V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5Gbps. Up to 6.5Gbps, you can connect this supply to either 3.0V or 2.5V.

For most applications, it is impractical to have a separate power supply for each voltage rail. Altera thus provides power-supply sharing guidelines. For example, Stratix V transceiver designs with data rates ≤ 6.5Gbps can generally use the configuration shown in **Figure 3**. This can require the SMPSs to supply up to 20A each at times.

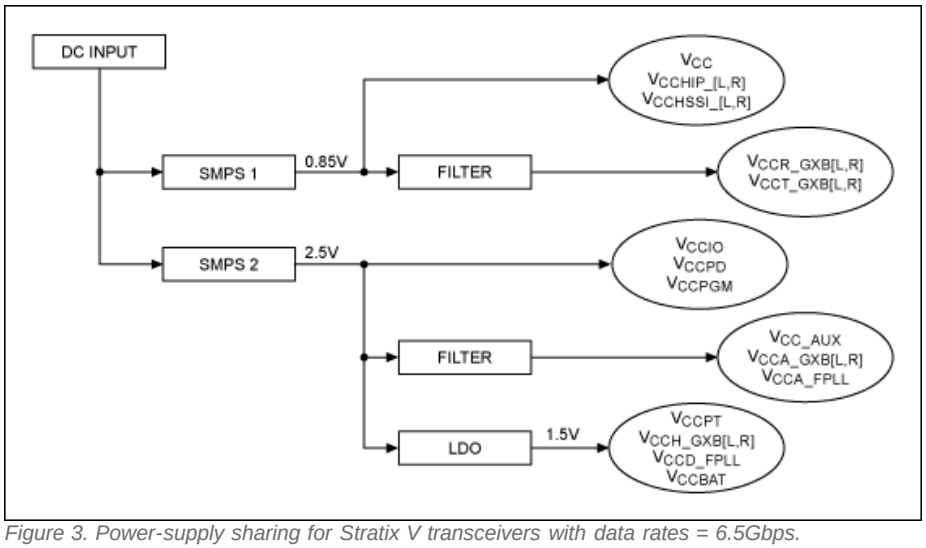


Figure 3. Power-supply sharing for Stratix V transceivers with data rates = 6.5Gbps.

FPGA manufacturers such as Altera often have software spreadsheets for estimating the power requirements of an FPGA device based on the required functionality of that FPGA. See www.altera.com/power for more information. Designers should use these spreadsheets in the early design stage to assist in selecting the appropriate power supply and thermal management components. **Table 2** shows an example of a power budget for the Stratix V setup shown in Figure 3. This power budget helps in determining the system efficiency and the required power regulator solution.

Table 2. Power Budget Calculations

V_{OUT} (V)		I_{OUT_MAX} (A)	P_{OUT} (W)	V_{IN} (V)	Efficiency (Estimated)	P_{IN}* = P_{OUT}/Eff.	I_{IN}* Required (A)	Power Dissipated (W)
V_{CC}, $V_{CCHIP\_[L,R]}$, $V_{CCHSSI\_[L,R]}$	0.85	3.0	2.55	5.0	0.93	2.74	0.55	0.19
$V_{CCR\_GXB[L,R]}$, $V_{CCT\_GXB[L,R]}$	0.85	2.0	1.7	5.0	0.93	1.83	0.36	0.13
V_{CCIO}, V_{CCPD}, V_{CCPGM}	2.5	0.7	1.75	5.0	0.95	1.84	0.37	0.09
V_{CCAUX}, $V_{CCA\_GXB[L,R]}$, V_{CCA_FPLL}	2.5	1.0	2.5	5.0	0.93	2.7	0.54	0.20

V_{CCPT}, $V_{CCH\_GXB[L,R]}$, V_{CCD_FPLL}, V_{CCD_BATT}	1.5	0.7	1.05	5.0	0.6	1.88	0.38	0.83
Total	9.55			10.99			2.2	1.44

*P_{IN} and I_{IN} are the power and current drawn from the DC input supply shown in Figure 3.

Power-Supply Considerations

In addition to using the power estimation tools to estimate the FPGA supply rail voltages and currents, there are several other aspects to choosing a power regulator. The following are some topics to consider.

Startup Sequencing/Tracking

Three or more voltage rails are typically required to power an FPGA. It is good design practice to implement sequencing for power-up and power-down between these rails. One advantage of this is that sequencing limits the inrush current during power-up. Also, even if the FPGA itself does not require sequencing, other devices in the design, such as microcontrollers and flash PROM, may have sequencing requirements. If the sequencing is ignored, the devices that require sequencing can be damaged or latchup, which in turn, can cause a malfunction.

There are three types of sequencing:

- Coincident tracking (also known as "simultaneous tracking")
- Sequential
- Ratiometric tracking

Figure 4 shows the different sequencing types and how the voltage rails rise in relation to each other.

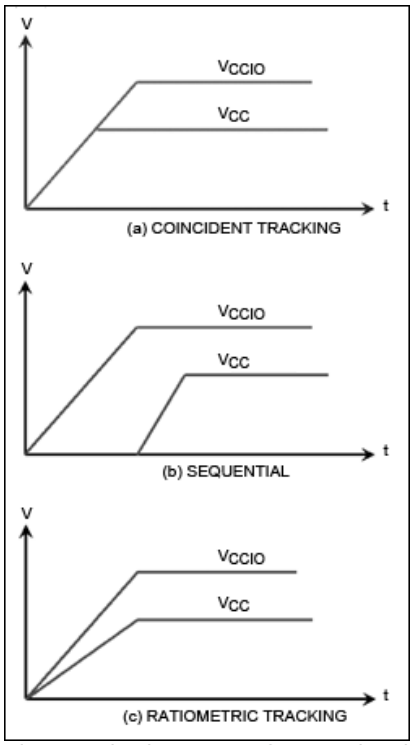


Figure 4. The three types of sequencing: (a) coincident tracking, (b) sequential, and (c) ratiometric tracking.

With coincident tracking, typically the preferred sequencing method for FPGAs, the rails ramp up simultaneously and at the same rate to their final set-points. This prevents unreliable startup due to latchup and bus contention. It also avoids turning on any parasitic conduction paths that could damage an FPGA. The higher startup inrush currents required by this type of sequencing

can require a larger capacitor bank to ensure that the rails rise monotonically. The inrush current issue is alleviated by the adjustable soft-start feature found on most of Maxim's POLs. For example, the MAX8686 facilitates coincident tracking and provides a programmable soft-start time based on the value of a single capacitor.

The main advantage with sequential sequencing is that it is generally easy to implement; startup inrush-current requirements are less than both coincident and ratiometric sequencing. However, the maximum voltage differential occurs between the voltage rails with this method, which could cause unreliable device behavior.

Ratiometric tracking ramps up all the voltage rails to reach their set-points at the same time. This reduces the voltage differential between the rails, compared to sequential sequencing. The level of startup inrush current is between the level for coincident tracking and sequential sequencing.

Monotonic Startup Voltage Ramping

It is important for the ramping voltage rails to rise monotonically at startup to achieve successful power-up. That means that they should rise continuously to their set-point and not droop. Drooping could result if the POL does not have enough output capacitance (**Figure 5**). The critical area for most FPGA core voltages is between 0.5V and 0.9V when the internal logic blocks are initialized to valid operating states.

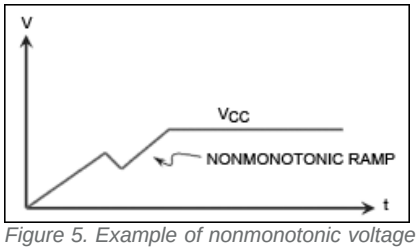


Figure 5. Example of nonmonotonic voltage ramp at startup.

Soft-Start

Most Altera FPGAs specify minimum and maximum startup ramp rates of 50µs and 100ms, respectively. However, there are exceptions. For example, the minimum ramp rate for the Stratix V is 200µs.

Power-supply regulators implement soft-start by gradually increasing the current limit at startup. This slows the rate of rise of the voltage rail and reduces the peak inrush current to the FPGA. Maxim's POLs allow soft-start times to be programmed based on the value of a soft-start capacitor connected to one of the POL pins.

Prebiased Startup

There are situations where an FPGA voltage rail remains biased at some voltage level when a power supply is shut down. This prebias is usually the result of various parasitic conduction paths through the FPGA. If the power supply restarts and pulls the prebiased output voltage low, it can result in unsuccessful startup of the FPGA. The output voltage of the power supply should instead be ramped up to its set-point, along with the other FPGA voltage rails in their desired sequence.

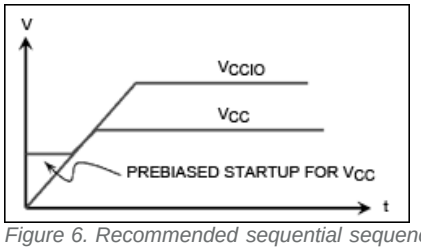


Figure 6. Recommended sequential sequencing startup for a prebiased output.

PCB Layout

While working on the PCB design, engineers must consider component placement, signal routing, and board layers. A multilayer board is highly recommended for FPGA designs, with a ground layer between each signal routing layer. The shielding that the ground layers provide allows for signal routing on every layer, without having to consider the adjacent routing layers. This facilitates a simpler and more practical layout.

Power-supply voltage and ground-plane placement in the PCB layer order (stackup) have a significant impact on the parasitic inductances of power current paths.

- High-priority voltage-supply layers should be placed closer to the component layer (in the top half of the PCB stackup). For example, power supplies with high-transient currents should have their associated voltage and ground planes close to the component layer. This decreases the via length (parasitic inductance) through which the high-transient currents must flow.
- Low-priority supplies should be placed farther from the component layer (in the bottom half of the PCB stackup).

Decoupling capacitors should be connected as close to the FPGA power pins as possible. The decoupling capacitors reduce any conducted noise from the power supply and radiated noise from surrounding circuits.

Some recommendations for the SMPS layout are:

- Minimize any parasitic inductance in the power-supply switched-current path by using short and wide traces between the critical components. This reduces the magnitude of voltage spikes that can be conducted and radiated into the FPGA.
- Place the regulator's decoupling capacitors as close to the regulator's IC pins as possible. Separate the power and analog ground planes.
- Keep the traces from the regulator's gate driver pins to the MOSFET gate pins short and wide to reduce the impedance seen by the gate-drive current.
- The high-current power-supply components that connect to the inner ground plane should use many ground vias to reduce the loop impedance.

See the MAX8686 data sheet for more layout information.

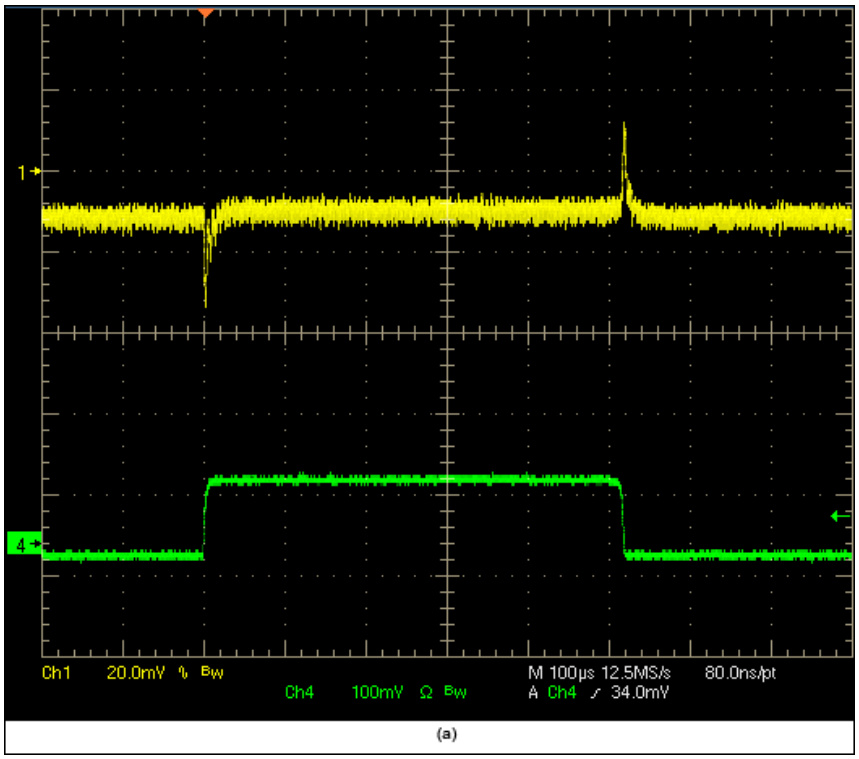
Power-Supply Transient Response

FPGAs can implement many functions at different frequencies due to their multiple clock domains. This can result in larger step changes in current requirements. The term "transient response" refers to a power supply's ability to respond to these abrupt changes in load current. A regulator should respond without significantly overshooting or undershooting its set-point and without sustained ringing in the output voltage. The transient response of a regulator depends on the following:

1. The speed at which the regulator's control loop responds when it detects a change in output voltage (or current, in the case of a current-mode controller).
2. The value and quality of output capacitance.

The control-loop unity-gain crossover frequency is typically designed to be 1/10 the regulator switching frequency. Thus, the regulator can be designed to respond quickly by operating at a high switching frequency (~1MHz).

The output capacitors should have very low effective series resistance (ESR) and be large enough to minimize the magnitude of the V_{OUT} transient overshoots and undershoots. Polymer capacitors provide the most capacitance with the lowest ESR. Ceramic capacitors have excellent high-frequency characteristics, but their total capacitance per device is one-half to one-quarter that of polymer capacitors. Typically, polymer or tantalum capacitors are used for the bulk output capacitance, while relatively low-value ceramic capacitors are placed at the FPGA input power pins for final stage filtering (**Figure 7**).



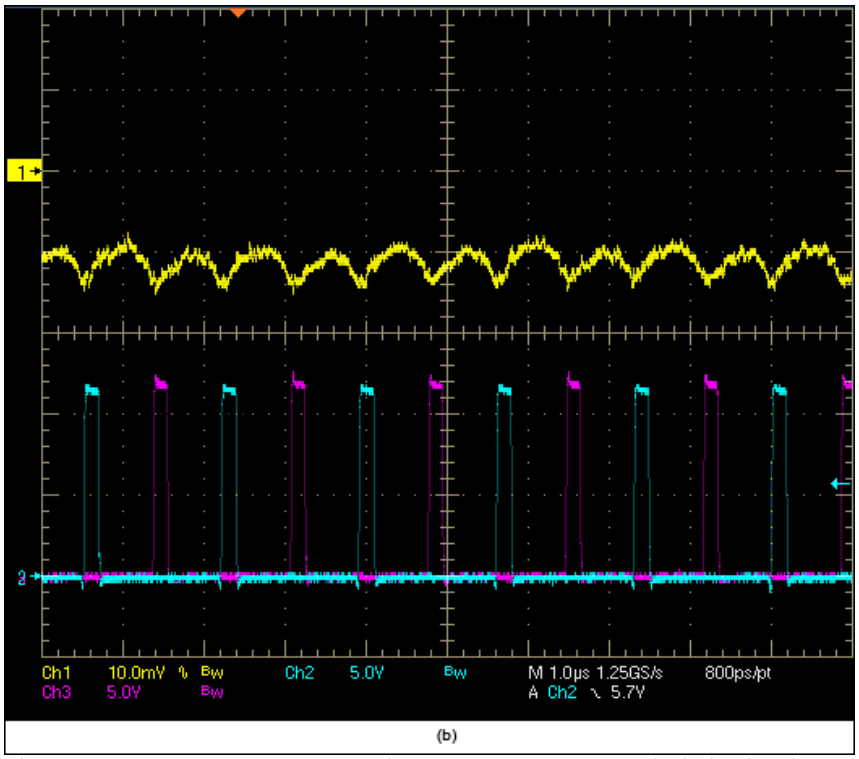


Figure 7. A 12V_{IN}, 1.2V_{OUT}-at-20A, 2-phase MAX8686 power-supply design for Altera FPGAs. (a) Transient response: 2A-to-12A load step with 22mV_{OUT} transients. (b) V_{OUT} ripple < 5mV at 5A_{OUT}.

Synchronizing to an External Clock

FPGAs applications usually require the power regulators to synchronize to a common clock. Many POLs provide an external SYNC pin to allow the system designer to synchronize one or multiple regulators to a common system clock.

Multiphase Operation

Multiphase regulators are essentially multiple regulators operating in parallel with their switching frequencies synchronized and phase shifted by 360/n degrees, where n identifies each phase. The advantages of designing with multiphase regulators become apparent as load currents rise above 20A to 30A. These advantages include:

1. A reduced input-ripple current, thus significantly decreasing the required input capacitance.
2. A reduced output-ripple voltage due to an effective multiplication of the ripple frequency.
3. A reduced component temperature, achieved by distributing the losses over more components.

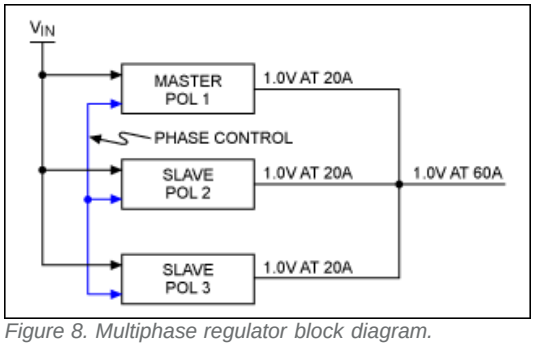


Figure 8. Multiphase regulator block diagram.

Remote Sensing

There can be a significant voltage drop between the power-supply output and the FPGA power-supply pins. This occurs particularly in applications where the load current is high and it is not possible to place the regulator circuit very close to the FPGA power pins. Remote sensing resolves this issue by using a dedicated pair of traces to accurately measure the voltage at the FPGA's power-supply pins (**Figure 9**). Remote sensing is also recommended for voltage rails with very tight tolerances (≤ 3%).

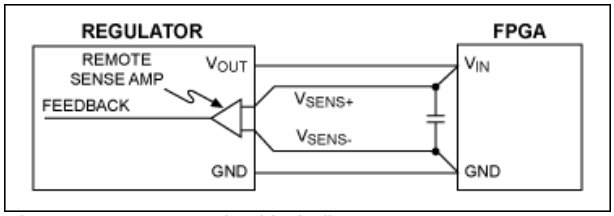


Figure 9. Remote-sensing block diagram.

Maxim's Power Solutions for Altera FPGAs

Maxim provides both LDO and SMPS regulators. SMPS regulators are typically selected to supply the higher-power FPGA voltage rails: The SMPSs produce better system efficiency and thermal management. Maxim's SMPS regulators offer a complete power-management solution where performance, power density, quality, and digital power management with accurate monitoring and control are required.

Maxim's power regulators include:

- PWM controllers
- PWM regulators—controllers with integrated MOSFETs and/or internal compensation and digital programming capability
- PMBus™ digital system control and monitoring
- Digital power control ICs

Synchronous PWM Controllers

Synchronous PWM controllers replace the external Schottky diode with a MOSFET to implement synchronous rectification, which improves efficiency. Synchronous PWM controllers can handle high current levels, since the switching MOSFETs are external to the controller ICs. Designers can select the most appropriate discrete MOSFETs for their particular current requirements.

Maxim provides a variety of synchronous PWM controllers for use with FPGAs. For example, the MAX15026 is a single controller, the MAX15023 is a dual controller, and the MAX15048/MAX15049 are triple controllers, all of which operate at up to $28V_{IN}$, making them suitable for $5V_{IN}$ and $12V_{IN}$ FPGA applications. Maxim also provides higher-voltage controllers (up to $40V_{IN}$), such as the MAX15046, for industrial and automotive applications. Most of Maxim's dual (or higher) controllers also have built-in sequencing and tracking that allow designers to use multirail ICs without requiring external sequencers.

PWM Regulators

Maxim's selection of PWM regulators facilitate output currents from 1A to 200A with input voltages ranging from 2.5V to 28V. The regulators have switching MOSFETs integrated with the PWM controllers. Examples include the MAX15053, MAX15041, and MAX8686. The MAX15021 and MAX17017 are multirail regulators that support dual and quad supply rails. Many of these ICs have popular fixed output-voltage options with fully internal compensation.

Some parts support digital programming, optional digital control, and monitoring functions that allow microsecond resolution programming of all timing events, such as sequencing and tracking. These extremely flexible monitoring features allow for intelligent settings of warning and fault thresholds. Independent setting of the fault-handling scenario for each regulator is also facilitated. Fine control of the output voltage with 0.2% accuracy will ensure meeting the tight tolerances of high-end FPGAs. Digital programmability and monitoring make field updates possible with a remote connection, and that helps avoid expensive field servicing. Additional benefits include the ability to log events so that failures can be studied and the root causes identified. A more comprehensive list of Maxim's POL regulators is given in our product guide, Analog Solutions for Altera FPGAs.

POL Digital System Control and Monitoring

Rack-based infrastructure equipment in communications and computing applications require sophisticated power management to turn on/off supplies and fans. Several customers building equipment for these markets use the Power Management Bus (PMBus™) protocol. The PMBus is an open-standard power-management protocol with a fully defined command language that facilitates communication with power converters and other devices in a power system. Maxim provides several PMBus monitors and system controllers. The MAX34440/MAX34441/MAX34446 are good examples of complex system PMBus monitors. These devices monitor the power-supply output voltages and constantly check for user-programmable overvoltage and undervoltage thresholds. The MAX34440 can manage up to six power supplies (**Figure 10**). The MAX34441 can monitor up to five power supplies and also contains a closed-loop fan-speed controller. Both the MAX34440 and MAX34441 can margin the power-supply output voltage up or down to a user-programmable level. The margining is performed in a closed-loop arrangement, in which the device automatically adjusts a pulse-width-modulated (PWM) output and then measures the resultant output voltage. The power-supply managers can also sequence the supplies in any order at both power-up and power-down. With the addition of an external current-sense amplifier (CSA), these devices can monitor currents.

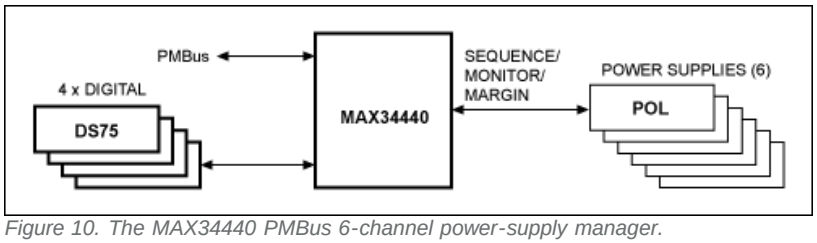


Figure 10. The MAX34440 PMBus 6-channel power-supply manager.

The MAX34446 power-supply data logger monitors voltages for overvoltage and undervoltage conditions, as well as for overcurrent and overtemperature conditions. The device constantly checks for user-programmable thresholds; when these thresholds are exceeded, the devices log the recent real-time operating conditions in nonvolatile flash memory (**Figure 11**). The devices can monitor up to four voltages or currents, and can monitor three temperature sensors.

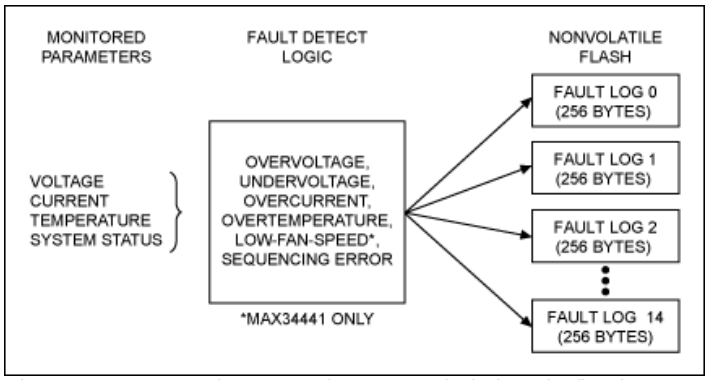


Figure 11. MAX34440/MAX34441/MAX34446 fault detection/logging.

The MAX8688 is an example of a fully integrated, digital power-supply controller and monitor that operates with any existing POL to provide complete digital programmability (**Figure 12**). By interfacing to the reference input, feedback node, and output enable, the MAX8688 takes control of the POL to provide functions such as tracking, sequencing, margining, and dynamic adjustment of the output voltage.

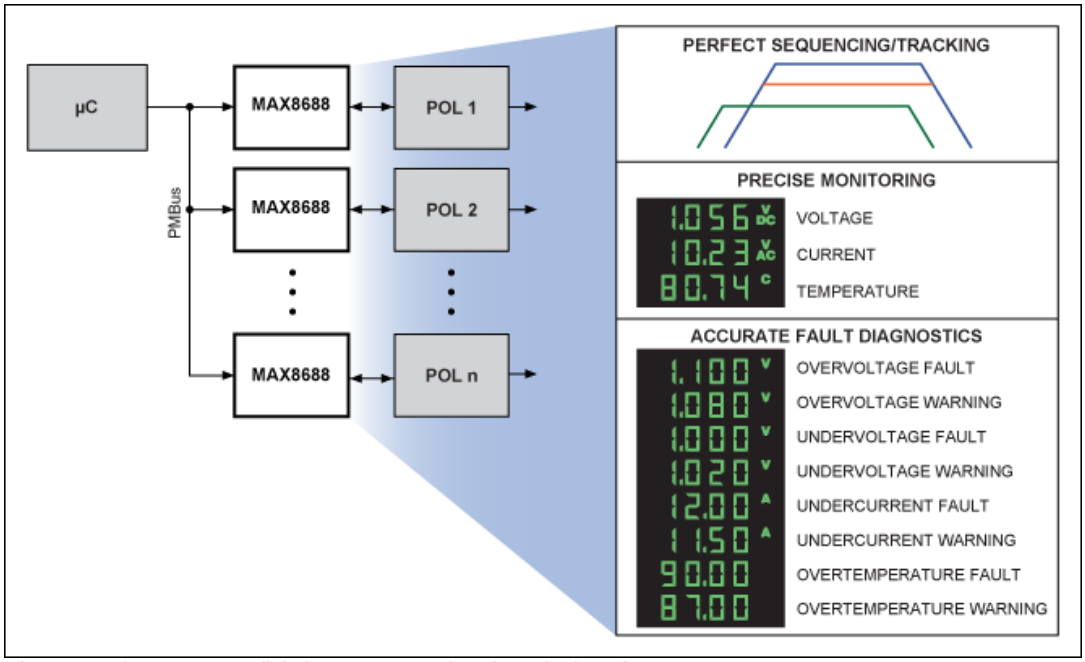


Figure 12. The MAX8688 digital system control and monitoring of POLs.

Digital Power-Control ICs

Historically, power-supply companies have focused on LDO and SMPS regulators. However, in complex infrastructure equipment that uses system-level power management, a more advanced digital control loop promises automatic compensation that is independent of output voltage. This advanced digital control loop results in design simplicity and dynamic power management. Unlike typical power regulators that use the analog control loop, digital power-control ICs (DPCs) use digital circuits to implement the control loop of a power supply. Customers requiring advanced system power management can benefit from a total solution cost advantage. Like the analog power regulators reviewed earlier in this document, these DPCs also have integrated on-chip digital power-management functionality that communicates to a system controller over the PMBus interface, facilitating easy power-supply design through a graphical user interface (GUI). The digital control loop ICs promise several benefits:

- **Shorter Time-to-Market**: Sophisticated DPCs can reduce design time by automatically compensating the control loop irrespective of output voltage. For customers who already benefit from internally compensated POLs with analog control, digital control takes it to the next level of ease of use.

- **Lower Cost**: DPCs decrease the number and size of components. The output capacitors can be reduced by up to 50%. Reliability is improved through the use of fewer components.
- **Improved Performance and Reliability**: The response to I_{OUT} transients is optimally controlled, resulting in lower V_{OUT} transients. The control algorithm improves efficiency by adjusting to voltage, current, and temperature variations.
- **Enhanced Flexibility**: DPCs simplify the system power-supply management. The system power supplies are controlled through the PMBus and additional power supplies can be easily added or removed for future system designs.

InTune™ Digital Power

Maxim's InTune digital-control power products make it easy to achieve high-performance DC-DC power-supply designs that require less filter capacitance and have greater efficiency. InTune digital power technology is based on "state-space" or "model-predictive" control, rather than the proportional-integral-derivative (PID) control used by competitors. The result is a faster transient response. Unlike competing PID controllers, the InTune architecture uses a feedback analog-to-digital converter (ADC) that digitizes the full output voltage range, thus eliminating the compromise associated with "windowed" ADCs used in competing controllers. Its automatic compensation routine is based on measured parameters, and provides better accuracy and efficiency over a wide range of operating conditions.

The MAX15301 in **Figure 13** is a full-featured, flexible, and efficient digital POL controller, based on InTune architecture, and with advanced power-management and telemetry features.

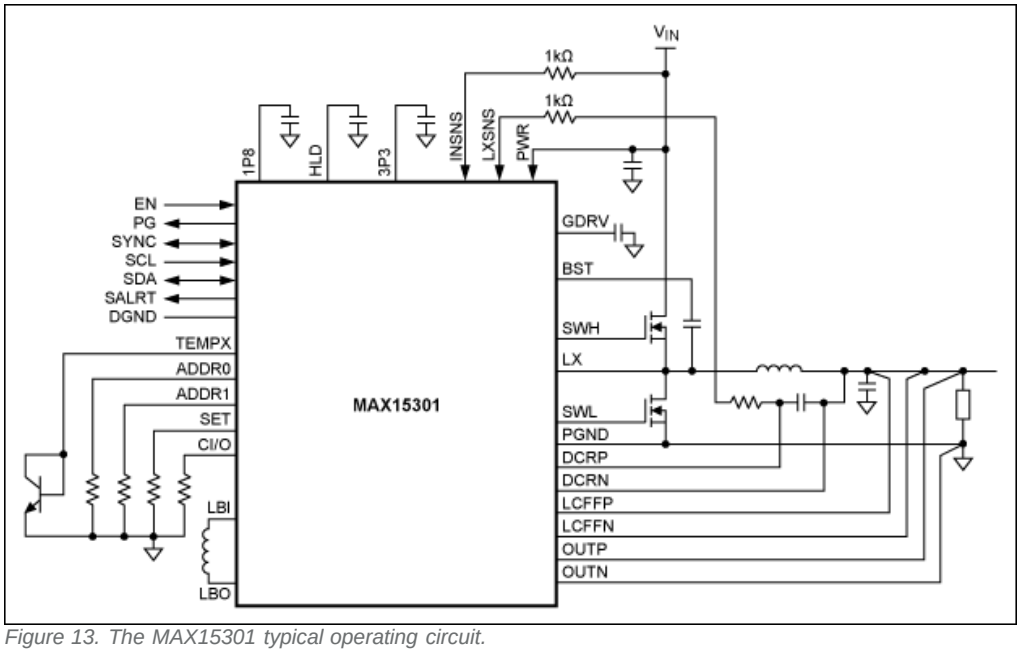


Figure 13. The MAX15301 typical operating circuit.

Table 3. Voltage Requirements for Common Altera FPGA/CPLD Voltage Supplies

FPGA	V_{CC}[1] (Tolerance)		V_{CCAUX}[2] (Tolerance)	V_{CCIO} (Tolerance)	V_{CCPD} (Tolerance)
Stratix V	0.85V (±30mV)		2.5V (±5%)	1.2V, 1.25V, 1.35V, 1.5V, 1.8V, 2.5V, 3.0V (±5%)	2.5V, 3.0V (±5%)
Stratix IV	0.90V[3] (±30mV)		2.5V (±5%)	1.2V, 1.5V, 1.8V, 2.5V, 3.0V (±5%)	2.5V, 3.0V (±5%)
Arria II	0.90V (±30mV)		see V_{CCPD}	1.2V, 1.5V, 1.8V, 2.5V, 3.3V (±5%)	2.5V, 3.0V, 3.3V (±5%)
Arria GX	1.20V (±50mV)		see V_{CCPD}	1.2V, 1.5V, 1.8V, 2.5V, 3.0V, 3.3V (±5%)	3.3 (±5%)
Cyclone IV E	1.0V (±30mV)	1.2V (±50mV)	2.5V (±5%)	1.2V, 1.5V, 1.8V, 2.5V, 3.0V, 3.3V (±5%)	—

Cyclone IV GX	1.2V (±40mV)			2.5V (±5%)	1.2V, 1.5V, 1.8V, 2.5V, 3.0V, 3.3V (±5%)	—
Cyclone III	1.20V (±50mV)			2.5V (±5%)	1.2V, 1.5V, 1.8V, 2.5V, 3.0V, 3.3V (±5%)	—
MAX V	1.8V (±5%)			—	1.2V, 1.5V, 1.8V, 2.5V, 3.3V (~ ±5%)	—
MAX II	3.3V (±300mV)	2.5V (±5%)	1.8V (±5%)	—	1.5V, 1.8V, 2.5V, 3.3V (~±5%)	—
Hardcopy IV	0.9V (±30mV)			2.5V (±5%)	1.2V, 1.5V, 1.8V, 2.5V, 3.0V (~ ±5%)	2.5V, 3.3V (±5%)

*Please check the corresponding device data sheet for the latest specifications.

Notes:

1. Some Altera devices refer to the core voltage supply as VCCINT.
2. VCCA for the Cyclone FPGAs.
3. The Stratix IV GT has a core voltage of 0.95 ±30mV.

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5. Stratix III Device Handbook, Volume 2
6. Stratix II Device Handbook, Volume 1
7. Arria II Device Handbook, Volume 3
8. Arria GX Device Handbook, Volume 1
9. Cyclone IV Device Handbook, Volume 3
10. Cyclone III Device Handbook, Volume 2
11. Cyclone II Device Handbook, Volume 1
12. HardCopy IV Device Handbook, Volume 4
13. HardCopy III Device Handbook, Volume 3
14. MAX V Device Handbook
15. MAX II Device Handbook
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18. Maxim application note 3177, "Powering High-Performance ASICs and Microprocessors."
19. Maxim PowerMind Brochure

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MAX1951	1MHz, All-Ceramic, 2.6V to 5.5V Input, 2A PWM Step-Down DC-to-DC Regulators	Free Samples
MAX1952	1MHz, All-Ceramic, 2.6V to 5.5V Input, 2A PWM Step-Down DC-to-DC Regulators	Free Samples
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MAX1971	Dual, 180° Out-of-Phase, 1.4MHz, 750mA Step-Down Regulator with POR and RSI/PFO	Free Samples
MAX1972	Dual, 180° Out-of-Phase, 1.4MHz, 750mA Step-Down Regulator with POR and RSI/PFO	Free Samples
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